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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,608	03/15/2001	James B. Johnson	MICS:0070	4991

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EXAMINER	
TRUJILLO, JAMES K	
ART UNIT	**PAPER NUMBER**
2116	2

DATE MAILED: 04/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/809,608	Applicant(s) JOHNSON ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: No papers have been received since the application was filed.

2. Claims 1-41 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-41 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shieh et al., U.S. Patent 6,003,118 (hereinafter "Shieh") in view of Keeth, U.S. Patent 6,016,282 (hereinafter Keeth).

5. As to claim 1, Shieh substantially teaches the claimed method comprising the acts:

a. providing a reference clock signal (external clock 22A) to a synchronization circuit (delay lock loop 22) coupled to an output data circuit (output buffer 24) configured to store the data being read from the memory device (DRAM Core 23) [figure 2.];

b. delaying the reference clock signal by the synchronization circuit to produce a output clock signal [col. 4 lines 50-52];

c. applying the output clock signal to the data output to remove the stored data therefrom synchronous with the reference clock signal [col. 1 lines 11-22].

Shieh does not expressly disclose *distorting* the reference clock and apply the *distorted* output clock signal to remove the data. In summary, Shieh taught delaying but not distorting the reference clock signal to provide synchronization of outputting data.

Keeth substantially teaches an adjustment circuit that distorts (adjusts the rising and falling edges of the clock signal) a reference clock signal (DCLK0) [col. 9 lines 58-64].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Shieh by incorporating the adjustment circuit as taught by Keeth because both invention are directed toward data timing in memory environments. One would have made the modification because Keeth teaches that the adjustment circuit would compensate for duty cycle variations [col. 2 lines 46-55].

6. As to claim 2, Shieh together with Keeth taught the method according to claim 1 described above. Shieh modified with the teachings of Keeth further taught wherein the reference clock comprises falling edges and rising edges, and wherein, when the distorted output clock signal is applied to the data output circuit, the stored data is removed therefrom synchronous with the falling and the rising edges of the reference clock signal [Shieh - col. 4 lines 37-59]. Shieh teaches that the memory system is a double data rated (DDR) SDRAM. A DDR requires that data be sent on both falling and rising edges of a clock.

7. A to claim 3, Shieh together with Keeth taught the method according to claim 1. Keeth further teaches wherein when the distorted output clock signal is applied to the data output circuit, the data output circuit generates a data output signal comprising data, the data output signal having reduced duty cycle distortion (compensating for effects of duty cycle variation resulting in accurately clocked data) [col. 2 lines 46-55].

8. As to claim 4, Shieh together with Keeth taught the method according to claim 3 described above. Shieh further substantially teaches wherein the data output signal has a 50% duty cycle [figure 4].

9. As to claim 5, Shieh together with Keeth taught the method according to claim 1 described above. Shieh together with Keeth further substantially teach determining an amount of distortion introduced by the data output circuit. Shieh together Keeth further substantially teach wherein the act of distorting the reference clock signal comprises distorting the reference clock signal in phase inverse relationship to the determined amount of duty cycle distortion. Specifically, both Shieh and Keeth teach using a DLL to compensate for delay and phase relationships of a clock. In particular, Shieh teaches using models of the output buffer and receiver in the DLL (28 and 29 in Figure 2). Keeth teaches determining the amount of distortion [col. 9 line 17 et seq.]. These delays and distortion are compensated by the modification of the DLL, taught by Shieh, and adjustment of rising and falling edges of the clock as taught by Keeth. The signals used for compensation must have a phase inverse relationship with the distortion because the delays and distortion are compensated.

10. As to claim 6, Shieh together with Keeth taught the method according to claim 5 described above. Shieh further teaches providing a model of the data output circuit (dummy output buffer 28) in a feedback path in the synchronization circuit [figure 2].

11. As to claim 7, Shieh together with Keeth taught the method according to claim 6 described above. Shieh further teaches wherein the model comprises a copy of the data output circuit (dummy output buffer 28) [figure 2].

12. As to claim 8, Shieh together with Keeth taught the method according to claim 7 described above. Shieh together with Keeth do not expressly disclose wherein the data output circuit comprises a latch. Shieh discloses using an output buffer. However, it would have been obvious to one of ordinary skill at the time of the invention to substitute the buffer for a latch. One of ordinary skill would have made the modification because a buffer and a latch provide the same function, that is, both temporarily hold data until ready. A latch provides the advantage in that it is easily implement with taking up less space.

13. As to claim 9, Shieh together with Keeth taught the method according to claim 1 described above. Keeth further taught wherein the reference clock signal comprises rising edges and falling edges, and wherein the act of delaying and distorting the reference clock signal comprises the acts of adjusting timing of the rising edges of the reference clock signal and adjusting timing of the falling edges of the reference clock signal [col. 10 lines 53-65].

14. As to claims 10 and 11, Shieh together with Keeth taught the method according to claim 1 described above. Claims 10 and 11 are further rejected for the same reasons as set forth hereinabove.

15. As to claims 12-41, Shieh together with Keeth taught the claimed method of reducing duty cycle distortion therefore they also taught the claimed method of reading data from a memory device, the claimed processor based device, the claimed delay lock loop and the claimed integrated circuit.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,584,021 to Heyne et al. This patent teaches using a DLL in a memory system.

U.S. Pat. No. 6,003,118 to Chen. This patent teaches using a PLL to access memory.

Japan Pat. No. JP411186903 to Ri. This patent teaches using a DLL with a memory device.

Hamamoto, T.; Kawasaki, S.; Furutani, K.; Yasuda, K.; Konishi, Y.; "A skew and jitter suppressed DLL architecture for high frequency DDR SDRAMs", VLSI Circuits, 2000. Digest of Technical Papers. 2000 Symposium on, 15-17 June 2000, Pages: 76 – 81. This paper teaches using DLL architecture in a memory system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
March 15, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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